IN THE CLAIMS

Please amend the claims as follows:

1-2. (Canceled)

3. (Previously Presented) The loss-of-signal detector of claim 10 wherein the predetermined delay ΔT is substantially equal to about ¼ of the recovered clock signal period T.

4. (Previously Presented) The loss-of-signal detector of claim 10 wherein the delay circuit comprises a buffer implemented in current-controlled complementary metal-oxide-semiconductor (C^3MOS) logic.

5. (Original) The loss-of-signal detector of claim 4 wherein the flip-flop is implemented in C^3MOS logic.

6. (Canceled)

7. (Previously Presented) The loss-of signal detector of claim 10 wherein the integrator comprises:

a current source configured to supply I_0;

a capacitor; and

a first switch coupled between the current source and the capacitor, and configured to open or close in response to the error signal generated by the flip-flop.

8. (Original) The loss-of-signal detector of claim 7 wherein the integrator further comprises a second switch coupled in parallel to the capacitor and configured to discharge the capacitor in response at the end of each integration period τint.

9. (Canceled)

10. (Previously Presented) In a receiver that includes a clock recovery circuit for extracting a recovered clock signal from an incoming data signal, a loss-of-signal detector comprising:

a delay circuit coupled to receive the incoming data signal and configured to shift a phase of the incoming data signal by a predetermined delay ΔT to generate a delayed data signal;

a flip-flop coupled to receive the recovered clock signal at one input and the delayed data signal at a second input;

an integrator coupled to an output of the flip-flop, wherein the integrator is configured to integrate a plurality of error signals generated by the flip-flop for an integration period, τint, and to generate a bit error rate sign, V_{BER};

a switch coupled to the integrator and configured to reset the integrator; and

a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage, wherein the comparator is configured to compare V_{BER} to a threshold level and to generate a loss-of-signal indicator when V_{BER} exceeds the threshold level,

wherein, the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal;

wherein the flip-flop is configured to generate an error signal when a transition of the delayed data signal falls outside the range $(T/2)\pm\Delta T$, where T is the period of the recovered clock signal,

and wherein the comparator comprises a hysteresis whereby the loss-of-signal indicator is asserted when V_{BER} exceeds a first threshold Vt1, and is not cleared until V_{BER} drops below a second threshold Vt2 that is lower than the first threshold Vt1.

11. (Original) The loss-of-signal detector of claim 7 wherein the first switch of the integrator comprises a pair of differentially coupled metal-oxide-semiconductor field effect transistors (MOSFETs).

12. (Currently Amended) The loss-of-signal detector of claim 11 wherein the pair of ~~MOSFET~~ MOSFETs are of p-channel type.

13. (Original) The loss-of-signal detector of claim 11 wherein the integrator further comprises a unity-gain buffer coupled between the pair of differentially coupled MOSFETs

14. (Currently Amended) In a receiver that includes a clock recovery circuit for extracting a recovered clock signal from an incoming data signal, a loss-of-signal detector comprising:

a delay circuit coupled to receive the incoming data signal and configured to shift a phase of the incoming data signal by a predetermined delay ΔT to generate a delayed data signal;

a flip-flop coupled to receive the recovered clock signal at one input and the delayed data signal at a second input;

an integrator coupled to an output of the flip-flop, wherein the integrator includes:

a current source;

a capacitor configured to be charged by the current source; and

a first switch coupled between the current source and the capacitor, and configured to open or close in response to the error signal generated by the flip-flop.

a second switch coupled in parallel to the capacitor and configured to discharge the capacitor in response at the end of each integration period τint,

and wherein the integrator is configured to integrate a plurality of error signals generated by the flip-flop for an integration period, τint, and to generate a bit error rate ~~sign~~ signal, V_{BER};

a divider circuit coupled to receive the recovered clock signal and configured to generate a signal representing the integration period τint;

a switch coupled to the integrator and configured to reset the integrator; and

a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage,

wherein, the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal;

wherein the flip-flop is configured to generate an error signal when a transition of the delayed data signal falls outside the range $(T/2)\pm\Delta T$, where T is the period of the recovered clock signal.

15-21. (Canceled)